

Paul V. Gratz

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| CONTACT INFORMATION | Department of Electrical and Computer Engineering 3259 TAMU, Texas A&M University College Station, TX 77843-3259 | Phone: (979) 488-4551 pgratz@gratz1.com http://www.gratz1.com/pgratz |
| RESEARCH INTERESTS | On-chip interconnection networks, high-performance multicore and distributed computer architecture, processor memory systems, VLSI design | |
| EDUCATION | The University of Texas , Austin, Texas USA Ph.D., Electrical and Computer Engineering, December 2008 <ul style="list-style-type: none">• Dissertation Topic: Network-On-Chip Implementation and Performance Improvement Through Workload Characterization and Congestion Awareness.• Dissertation Advisor: Dr. Stephen W. Keckler.• Area of Study: Computer Architecture, Computer Engineering. The University of Florida , Gainesville, Florida USA M.S., Electrical and Computer Engineering, August 1997 <ul style="list-style-type: none">• Area of Study: Digital Signal Processing. B.S., Electrical and Computer Engineering, August 1994 <ul style="list-style-type: none">• Physics Minor. | |
| HONORS | <ul style="list-style-type: none">- Best papers of IEEE Computer Architecture Letters in 2011, “B-Fetch:Branch Prediction Directed Prefetching for In-Order Processors”, IEEE Computer Architecture Letters, Jan. 2012- Teaching Excellence Award, Texas A&M University System, Teaching Excellence Award Program - Top 5%, Spring 2010.- Best Paper Award, “An Evaluation of the TRIPS Computer System”, ASPLOS 2009.- Engineering Doctoral Fellowship, UT College of Engineering, 2003–2005.- Elected Member, Tau Beta Pi. | |
| EXPERIENCE | Texas A&M University , College Station, Texas USA <i>Assistant Professor</i> 2009 – present Department of Electrical and Computer Engineering Research Interests: <ul style="list-style-type: none">• On-chip interconnection networks.• High performance multicore and distributed computer architectures.• Processor memory systems. The University of Texas , Austin, Texas USA <i>Graduate Research Assistant</i> 2003 – 2008 Computer Architecture and Technology Research (CART) Lab <ul style="list-style-type: none">• Researched use of network status information to improve network-on-chip performance.• Led development of TRIPS prototype processor’s second-level cache system, a static NUCA implementation, and inter-processor interconnection networks. | |

- Developed the TRIPS processor RTL CAD environment, design methodology and RTL database, a 170 million transistor prototype in 130nm ASIC technology.

Graduate Teaching Assistant **Aug. 2007 – Dec 2007**
 Department of Computer Science

- TA for honors undergraduate computer architecture class.
- Students of this course gain practical experience computer architecture through the design, implementation and synthesis of a simple RISC microprocessor.
- Guest lectured, held office hours, and graded papers and exams.

Intel Corp., Austin, Texas USA **2000 – 2002**
Design Automation Engineer
 Tejas Project

- Developed and supported RTL database build scripts to build full-chip verilog model using Synopsys VCS.
- Developed and supported validation test-running tools to support massive parallel runs of tests in a batched network environment.

Intel Corp., Chandler, Arizona USA **1998 – 2000**
Design Engineer
 Arizona Development Company

- Developed and supported logic verification tools for the Itanium project.
- Performed logic verification on the Itanium full chip model.
- Uncovered initialization problems by comparing schematics and RTL using logic validation tools.
- Circuit design of the Itanium CPU ID fuse unit.

Design Engineer **1997 – 1998**
 Rotational Engineering Program

- Performance evaluation of the Strongarm 1100 microprocessor.
- Logic verification on the debug (DBG), performance monitoring (PMU), and in-test circuit (ITC) units of the Itanium processor.
- Architecture validation on an i960 derivative microprocessor.

The University of Florida, Gainesville, Florida USA **1995 – 1997**
Graduate Teaching Assistant
 Department of Electrical and Computer Engineering

- TA for graduate and undergraduate, computer architecture hardware design labs.
- TA for undergraduate logic design lab.
- TA for senior design project lab.

REFEREED
 CONFERENCE
 PUBLICATIONS

“Energy-efficient Optical Broadcast for Nanophotonic Networks-on-Chip”, C. Li, M. Browning, P. V. Gratz and S. Palermo. *The 2012 IEEE Optical Interconnects Conference (OIC)*, May 2012. (Accepted for publication)

“In-Network Monitoring and Control Policy for DVFS of CMP Networks-On-Chip and Last Level Caches”, Xi Chen, Zheng Xu, Hyungjun Kim, Paul Gratz, Jiang Hu, Michael Kishinevsky and Umit Ogras. *The Sixth ACM/IEEE International Symposium on Networks-on-Chip (NOCS)*, May 2012. (Accepted for publication)

“Exploiting Path Diversity for Low-Latency and High-Bandwidth with the Dual-path NoC Router,” Y. S. Yang, H. Deshpande, G. Choi and P. V. Gratz. *The 2012 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2012. (Accepted for publication)

“Reducing Network-on-Chip Energy Consumption Through Spatial Locality Speculation,” H. Kim, P. Ghoshal, B. Grot, P. V. Gratz and D. A. Jiménez. *The Fifth ACM/IEEE International Symposium on Networks-on-Chip (NOCS)*, May 2011. Acceptance rate: 25%

“AcENoCs: A Configurable HW/SW Platform for FPGA Accelerated NoC Emulation,” V. Pai, S. Lotlikar, and P. V. Gratz. *The 24th IEEE International Conference on VLSI Design (VLSID)*, Jan. 2011. Acceptance rate: 20%

“Asynchronous Bypass Channel Routers: Improving Performance for DVFS and GALS NoCs,” T. Jain, P. V. Gratz, A. Sprintson, and G. Choi. *The 4th IEEE/ACM International Symposium on Networks-on-Chips (NOCS)*, May 2010. Acceptance rate: 27%

“An Evaluation of the TRIPS Computer System”, M. Gebhart, B. A. Maher, K. E. Coons, J. Diamond, P. Gratz, M. Marino, N. Ranganathan, B. Robotmili, A. Smith, J. Burrill, S. W. Keckler, D. Burger, K. S. McKinley. *The 14th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, March 2009. Best Paper Award, Acceptance rate: 25.7%

“Regional Congestion Awareness for Load Balance in Networks-on-Chip”, P. Gratz, B. Grot, and S.W. Keckler. *The 14th IEEE International Symposium on High-Performance Computer Architecture (HPCA)*, February 2008. Acceptance rate: 19%

“TRIPS: A Distributed Explicit Data Graph Execution (EDGE) Microprocessor”, M.S. Govindan, K. Sankaralingam, R. Nagarajan, R. McDonald, R. Desikan, S. Drolia, P. Gratz, D. Gulati, H. Hanson, C.K. Kim, H. Liu, N. Ranganathan, S. Sethumadhavan, S. Sharif, P. Shivakumar, S.W. Keckler, and D. Burger, *HotChips 19*, August 2007.

“Implementation and Evaluation of a Dynamically Routed Processor Operand Network”, P. Gratz, K. Sankaralingam, H. Hanson, P. Shivakumar, R. McDonald, S.W. Keckler, and D.C. Burger. *The First IEEE International Symposium on Networks-on-Chips (NOCS)*, pp. 7–17, May 2007. Acceptance rate: 27%

“Distributed Microarchitectural Protocols in the TRIPS Prototype Processor”, K. Sankaralingam, R. Nagarajan, R. McDonald, R. Desikan, S. Drolia, M.S. Govindan, P. Gratz, D. Gulati, H. Hanson, C. Kim, H. Liu, N. Ranganathan, S. Sethumadhavan, S. Sharif, P.K. Shivakumar, S. W. Keckler, D.C. Burger. *The 36th IEEE/ACM International Symposium on Microarchitecture (MICRO)*, pp. 480–491, December 2006. Acceptance rate: 24%

“Implementation and Evaluation of On-Chip Network Architectures”, P. Gratz, C. Kim, R. McDonald, S.W. Keckler, and D.C. Burger. *2006 IEEE International Conference on Computer Design (ICCD)*, pp. 477–484 October 2006.

“B-Fetch:Branch Prediction Directed Prefetching for In-Order Processors”, R. Panda, P.V. Gratz and D. A. Jiménez. *IEEE Computer Architecture Letters*, 11/29/11 (Rapid-Posts). *Acceptance rate: ~24% Best papers of IEEE Computer Architecture Letters in 2011*

“Asynchronous Bypass Channels for Multi-synchronous NoCs: A Router Microarchitecture, Topology and Routing Algorithm”, T.N.K. Jain, M. Ramakrishna, P.V. Gratz, A. Sprintson and G. Choi. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol.30, no.11, pp.1663-1676, Nov. 2011.

“The TRIPS OPN: A Processor Integrated NoC for Operand Bypass”, P.V. Gratz, S.W. Keckler, *Designing Network On-Chip Architectures in the Nanoscale Era*, edited by J. Flich and D. Bertozzi, CRC Press, Dec. 2010.

“Leveraging Unused Cache Block Words to Reduce Power in CMP Interconnect”, H. Kim, P. V. Gratz, *IEEE Computer Architecture Letters*, **9**, pp. 33-36, January-June 2010. *Acceptance rate: 24%*

“An Evaluation of the TRIPS Computer System”, M. Gebhart, B. A. Maher, K. E. Coons, J. Diamond, P. Gratz, M. Marino, N. Ranganathan, B. Robotmili, A. Smith, J. Burrill, S. W. Keckler, D. Burger, K. S. McKinley. *ACM SIGPLAN Not.* 44, 3 (March 2009), 1-12.

“Architecture and Implementation of the TRIPS Processor”, S.W. Keckler, D. Burger, K. Sankaralingam, R. Nagarajan, R. McDonald, R. Desikan, S. Drolia, M.S. Govindan, P. Gratz, D. Gulati, H. Hanson, C. Kim, H. Liu, N. Ranganathan, S. Sethumadhavan, S. Sharif, and P. Shivakumar, *Unique Chips and Systems*, edited by E. John and J. Rubio, CRC Press, 2007.

“On-Chip Interconnection Networks of the TRIPS Chip”, P. Gratz, C. Kim, K. Sankaralingam, H. Hanson, P. Shivakumar, S.W. Keckler, and D.C. Burger. *IEEE Micro*, **27**(5), pp. 41-50, September/October 2007.

“Scaling to the End of Silicon with EDGE Architectures”, D.C. Burger, S.W. Keckler, K.S. McKinley, et al. *IEEE Computer*, **37**(7), pp. 44-55, July, 2004.

“An Energy Efcient Datapath for Asymmetric Cryptography”, A.D. Targhetta and P.V. Gratz, *The 3rd Workshop on Energy Efficient Design (WEED 2011)*, June 2011.

“Ocin_tsim - a DVFS aware simulator for NoC based platforms”, S. Prabhu, B. Grot, P. V. Gratz and J. Hu, *The 1st Workshop on SoC Architecture, Accelerators and Workloads (SAW-1)*, January 2010.

“Realistic Workload Characterization and Analysis for Networks-on-Chip Design”, P. V. Gratz and S. W. Keckler. *The 4th Workshop on Chip Multiprocessor Memory Systems and Interconnects (CMP-MSI)*, January 2010.

“Running PARSEC 2.1 on M5”, M. Gebhart, J. Hestness, E. Fatehi, P. Gratz, S. W. Keckler. *Technical Report: #TR-09-32*, The University of Texas at Austin, Department of Computer Science. October 27, 2009.
http://www.cs.utexas.edu/~cart/parsec_m5/

“Asynchronous Bypass Channel Routers,” T. Jain, P. V. Gratz, A. Sprintson, and G. Choi, *Technical Report:TAMU-ECE-2009-05*, August 24, 2009.

PATENTS

“Congestion-Aware Routing in a Computer Interconnection Network”, with P. V. Gratz, S. W. Keckler and B. Grot, US Provisional Patent, DW Docket Number: 190607/US, filed February 2009.

“Method and Apparatus for Providing Dynamic Composition of Multiple Processor for Adaptive Single- Threaded Execution”, with S. Keckler, D. Burger, N. Ranganathan, S. Sethumadhavan, K. Sankaralingam, R. Nagarajan, C. Kim, P. V. Gratz, and H. Liu, US Provisional Patent, filed June, 2007.

PRESENTATIONS

Columbia University, “Directed Speculation in Multi-core Memory Systems to Improve Efficiency and Performance,” invited seminar for the Computer Engineering Group of the Department of Computer Science, November 2011.

The University of Texas at Austin, “Improving Synthetic Workloads for NetworkOnChip Design and Analysis Through Realistic Workload Characterization ,” invited seminar for the Laboratory for Computer Architecture (LCA), February 2009.

“Implementation and Evaluation of a Dynamically Routed Processor Operand Network,” *The First IEEE International Symposium on Networks-on-Chips* (NOCS), May 2007.

“Implementation and Evaluation of On-Chip Network Architectures,” *2006 IEEE International Conference on Computer Design* (ICCD), October 2006.

“Chip- and system-level networks and I/O in the TRIPS Prototype,” TRIPS Tutorial: Design and Implementation of the TRIPS EDGE Architecture

- *The 12th IEEE International Symposium on High-Performance Computer Architecture* (HPCA), February 2006.
- *The 32nd International Symposium on Computer Architecture* (ISCA), June 2005.

PROFESSIONAL
ACTIVITIES

Reviewer for the following conferences and journals: ASPLOS 2009, 2008, 2004, ACM TACO 2009, ACM TECS 2011, ACM TODAES 2011, HPCA 2011, IEEE CAL 2011, 2010, 2009, 2008, IEEE Micro 2011, IEEE TC 2011, 2010, 2009, IEEE TCAD 2010, IEEE TVLSI 2011, 2010, IISWC 2006, IPDPS 2005, JCST 2011, JPDC 2010, Micro 2011, 2006, MICROPRO 2010, SC 2011

Program Committees: IEEE MEDEA 2009, IEEE IISWC 2011, IEEE IPDPS 2012, IEEE NOCS 2012.

Organizing Committees: IEEE HPCA 2011 - Publication Chair, IEEE IISWC 2011 - Publication Chair

Member, IEEE (Computer Society)

Member, ACM (SIGARCH)

PERSONAL
INFORMATION

Date of Birth: 18th August, 1970

Citizenship: US Citizen